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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/029,608	05/15/98	FUKASAWA	N 980233

EXAMINER	
GRAYBILL, D	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/029,608	Applicant(s) FUKASAWA ET AL.
	Examiner David E Graybill	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,19,36,41-43,87-91,95-102 and 109-131* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,19,36,41-43,87-91,95-102 and 109-131* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *29-31* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 110, 116, 117 and 129 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly the subject matter which applicant regards as the invention.

There is insufficient literal antecedent basis for the following:

Claim 116, "the elastic resin";

Claim 117, "the protruding core portion";

Claim 129, "the side surface."

Claim 110 is rejected as incomplete because it depends on canceled claim 108.

116 has not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejection supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claim; hence, it would not be proper to reject the claim on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions

that must be made as to the scope of the claims. See also MPEP 2173.06.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 18, 19, 36, 41, 43, 87-91 and 97-102 are rejected under 35 U.S.C. 102(e) as being anticipated by Kata (5897337).

At column 4, line 8 to column 14, line 50, Kata teaches the following:

18. A semiconductor device comprising: a semiconductor element 50 having a surface on which electrode pads 41 connected to an internal part of the semiconductor element and protruding electrodes 66 to be connected to an external part are formed; lead lines 62 each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and a resin layer 61/43 which is formed on the surface of the semiconductor element and seals at least a lateral surface of

the protruding electrodes; wherein the lead lines are located between the semiconductor element and the resin layer.

19. The semiconductor device as in 18, further comprising a heat radiating member 46 provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

36. A semiconductor device comprising: a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and external connection electrodes are provided which are to be electrically connected to external terminals; lead lines each connecting one of the electrode pads and one of the external connecting electrodes so that the external connecting electrodes and the internal part are connected through the lead lines; and a resin layer provided on the surface of the semiconductor element so as to cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the resin layer and the lead lines are located between the semiconductor element and the resin layer.

41. The semiconductor device as in 18, wherein the resin layer comprises a plurality of resin layers having different characteristics.

43. A semiconductor device comprising: a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected, through the lead lines; a resin layer which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and external connection protruding electrodes 67 provided to the ends of the protruding electrodes exposed from the resin layer; wherein the lead lines are located between the semiconductor element and the resin layer.

87. A semiconductor wafer on which semiconductor elements are provided, comprising: a semiconductor wafer 50 including a plurality of semiconductor elements having a surface on which electrode pads 41 connected to an internal part of the semiconductor elements and protruding electrodes 66 to be connected to an external part are formed; lead lines 62 each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines and a resin layer 61/63 which is formed on the surface of the semiconductor elements and seals at

least a lateral surface of the protruding electrodes; wherein the lead lines are located between the semiconductor elements and the resin layer.

88. A semiconductor device comprising: a semiconductor element having a surface on which, electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part ate formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and a resin layer which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes, wherein a lateral surface of the resin layer and a lateral surface of the semiconductor element have planes cut by a dicer, and the lead lines are located between the semiconductor element and the resin layer.

89. A semiconductor device as in 88, wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have a common plane cut by a dicer.

90. A semiconductor device comprising: a semiconductor element having a surface on which external connection electrodes are provided, which are to be electrically connected to external terminals; and a compressed resin layer provided on the surface

of the semiconductor elements so as to cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the compressed resin layer, the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer.

91. A semiconductor device comprising: a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and a resin layer which is formed on the surface on the semiconductor element and seals a lateral surface and a top of the protruding electrodes, the resin layer slightly covering upper portions of the protruding electrodes; wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer and the lead lines are located between the semiconductor element and the resin layer.

97. The semiconductor device as in 88, wherein the [compressed] resin layer is formed by disposing a film between the protruding

electrodes and a mold, which thus contacts the resin layer through the film.

98. The semiconductor device as in 88, wherein a sheet-shaped resin is used as the resin layer.

99. The semiconductor device as in 88, wherein a reinforcement plate is loaded onto a mold before the substrate is loaded onto the mold in forming the resin layer.

100. The semiconductor device as in 88, wherein: a film used in forming the resin layer is formed of an elastically deformable substance, and ends of the protruding electrodes are caused to fall in the film when the resin layer is formed by using a mold; and the film is detached from the resin layer when the protruding electrodes are exposed so that the ends of the protruding electrodes can be exposed from the resin layer.

101. The semiconductor device as in 88, further comprising a heat radiating member provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

102. The semiconductor device as in 88, wherein the resin layer comprises a plurality of sealing resins having different characteristics.

To further clarify the teaching of a plurality of resin layers having different characteristics, it is noted that the layers have different location characteristics.

To further clarify the teaching of a compressed resin layer 43, it is noted that Kata teaches this product at column 8, lines 23-24; and column 9, lines 37-43 because the resin layer is inherently compressed when the film is pressed.

To further clarify the teaching of a resin layer 43 which seals a top of the protruding electrodes, it is noted that the resin layer seals a top of the lateral surface of the electrode. In any case, there is no absolute frame of reference recited; therefore, it is inherent that for any particular sealed portion of the electrode, an absolute frame of reference can be chosen in which the portion is a top of the electrode.

To further clarify the teaching of the resin layer covering upper portions of the protruding electrodes, attention is directed to figure 8D wherein the resin layer slightly covers the upper portions of the protruding electrodes that slightly overlap the external surface of the layer.

Also, although Kata does not appear to explicitly teach the process limitations of claims 88-91, 97, 99 and 100, the product of Kata inherently possesses the structural characteristics

imparted by the limitations. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claim 42 is rejected under 35 U.S.C. 102(b) as being anticipated by Kata (5683942).

At column 3, line 34 to column 10, line 47, Kata teaches the following:

42. A semiconductor device comprising: a semiconductor element 1 having a surface on which electrode pads 2 connected to an internal part of the semiconductor element and protruding electrodes 4/9 to be connected to an external part are formed; lead lines 6 each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines, and a first resin layer 3 that is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and a second resin layer 53 provided so as to cover at least a back surface of the semiconductor element; wherein the lead lines are located between the semiconductor element and the resin layers.

Claims 95 and 96 are allowed.

Claims 109, 111-114, 117, 118, 121-123 and 131 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasunaga (5656863).

At column 1, line 1 to column 2, line 5; column 3, lines 7-47; column 16, line 16 to column 18, line 12; and column 25, lines 44-47, Yasunaga teaches the following:

109. A semiconductor device comprising: a semiconductor element 113 having a surface on which protruding electrodes 112 are formed; a resin layer 111 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and external connection protruding electrodes 115 provided to the end portions of the protruding electrodes that protrude from the resin layer.

111. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 112 having convex end portions are formed; a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except the convex end portions thereof; and external connection protruding electrodes provided to the convex end portions of the protruding electrodes that protrude from the resin layer.

112. The semiconductor device as in 111, wherein the resin layer and the semiconductor element have surfaces.

113. A semiconductor device comprising a semiconductor element having a surface on which protruding electrodes are formed; and a resin layer formed on the surface of the semiconductor element

so as to seal the protruding electrodes except end portions thereof, the protruding electrodes having a core portion 112 and an electrically conductive film formed on a surface of the protruding core portion.

114. The semiconductor device as in 113, wherein an end portion of the electrically conductive film on a side on which the semiconductor element is located is electrically connected to the semiconductor element.

117. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes are formed; a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and external connection protruding electrodes provided to the end portions of the protruding electrodes that protrude from the resin layer, the protruding electrodes having a core portion and an electrically conductive film formed on a surface of the protruding core portion.

118. The semiconductor device as in 117, wherein an end portion of the electrically conductive film on a side on which the semiconductor element is located is electrically connected to the semiconductor element.

121. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes are formed; and

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, the semiconductor element having an outer peripheral portion that is thinner than a central portion thereof.

122. A semiconductor device comprising a semiconductor element having a surface on which protruding electrodes are formed; and a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, the semiconductor element having an outer peripheral portion that is thicker than a central portion thereof.

123. A semiconductor device comprising a semiconductor element having a surface on which protruding electrodes are formed; and a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof, a part of a side portion of the semiconductor element being covered with the resin layer.

131. A semiconductor device comprising: a semiconductor element 3 having a surface on which protruding electrodes 9, 10 are formed; a compression-molded resin layer 1 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof ("top surface of the first conductor 9"); and external connection protruding electrodes 10 provided to the end portions of the protruding

electrodes that protrude from the compression-molded resin layer, the compression-molded resin layer and the semiconductor element having surfaces.

To further clarify the teachings of the semiconductor element having an outer peripheral portion that is thinner than a central portion thereof, and the semiconductor element having an outer peripheral portion that is thicker than a central portion thereof, it is noted that the element 113 has an outer external horizontal peripheral portion that is thicker than a central internal vertical portion, and an outer external vertical peripheral portion that is thinner than a central internal horizontal portion.

To further clarify the teaching of a part of a side portion of the semiconductor element being covered with the resin layer, it is noted that the top side portion of the element is covered with the resin layer.

Also, although Yasunaga does not appear to explicitly teach the process limitation, "wherein the resin layer and the semiconductor element have surfaces defined by cutting using a dicer," the product of Yasunaga inherently possesses the structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claims 115, 119 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasunaga as applied to claims 109, 111-114, 117, 118, 121-123 and 131 and further in combination with Nolan (5508228).

Yasunaga does not appear to explicitly teach the following:

115. The semiconductor device as in 113, wherein the core portion comprises an elastic resin.

119. The semiconductor device as in 117, wherein the core portion comprises an elastic resin.

120. The semiconductor device as in 119, wherein the elastic resin is polyimide.

Nevertheless, at column 5, line 26 to column 7, line 60, Nolan teaches wherein a core portion 24 comprises an elastic polyimide resin. In addition, it would have been obvious to combine the product of Nolan with the product of Yasunaga because it would provide an electrode.

Claims 124-130 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishino (JP555278).

In the English abstract and figures, Nishino teaches the following:

124. A semiconductor device comprising: a semiconductor element 1 having a surface on which protruding electrodes 5 are formed; a resin layer 3 formed on the surface of the semiconductor

element so as to seal the protruding electrodes except end portions thereof; and a protrusion 5 for positioning of the semiconductor device, the protrusion being formed on the surface of the semiconductor device and having an end portion exposed from the resin layer.

125. The semiconductor device as in 124, wherein the resin layer and the semiconductor element have surfaces defined by cutting using a dicer.

126. The semiconductor device as in 124, wherein the protrusion for positioning has a structure identical to that of the protruding electrodes.

127. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes are formed; and a molded resin layer 3 formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof.

128. The semiconductor device as in 127, wherein the compression-molded resin layer and the semiconductor element have surfaces defined by cutting using a dicer.

129. The semiconductor device as in 128, wherein the side surface of the resin layer and the side surface of the semiconductor element are flush with each other.

130. The semiconductor device as in 127, wherein end portions of the protruding electrodes protrude from the compression-molded resin layer.

To further clarify the teaching wherein the side surface of the resin layer and the side surface of the semiconductor element are flush with each other, it is noted that the sides of the resin layer and surface of the semiconductor that interface in direct contact are directly abutting and immediately adjacent each other; therefore, they are flush with each other.

Also, although Nishino does not appear to explicitly teach the process limitation "compression-molded," the product of Nishino inherently possesses the structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Applicant's amendment and remarks filed 7-30-01 are addressed in the rejection supra and are further addressed infra.

Applicant argues that Kata '337 does not teach wherein the lead lines are located between the semiconductor element and the resin layer. This argument is respectfully traversed because Kata clearly teaches that the lead lines are located between the element and the resin layer portion 61.

Also, applicant suggests that Kata '942 does not teach that resin layer 3 is formed on the surface of the semiconductor element. This suggestion is respectfully traversed because Kata clearly teaches that the layer is formed at a position in and/or in close proximity with the surface of the element; therefore, it is formed on the element.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.
17-Oct-01